



MICROCOMPUTERS

**Users' Manual
Memory Expansion Module
KIM-3B**

MOS TECHNOLOGY INC.
230 Franklin Road
Menlo Park, CA 94025

Users' Manual

Memory Expansion Module

KIM-3B

The information in this manual has been reviewed and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. The material in this manual is for informational purposes only and is subject to change without notice.

First Edition
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MOS TECHNOLOGY, INC.
950 Rittenhouse Road
Norristown, PA. 19401

CHAPTER 1
Introduction

Congratulations on your purchase of a KIM memory expansion board. It has been carefully engineered to provide high reliability and a long service life. Please make sure you take a few minutes and read this User's Manual completely. You will then be familiar with all the features of your memory expansion board and will find it easy to connect the board to your existing KIM-1 system.

A single memory expansion board may be wired directly to your KIM-1. By using the KIM-4 motherboard you may add additional memory modules to expand your memory space by an additional 58,000 bytes

Like all MOS Technology, Inc. microprocessor modules, your memory expansion module is completely assembled and tested. Even if you are not using a KIM-4 motherboard, all you will have to do is wire a simple cable. Your KIM memory expansion module is covered by a complete 90-day warranty and, like all KIM modules, factory repair services are available even after the expiration of your warranty.

Your KIM memory expansion board has its own +5v regulator and requires only 8 to 10 VDC unregulated for satisfactory operation. If you already have a regulated +5v supply, you may use it with your expansion board and bypass the regulation circuitry.

All the necessary circuitry has been included to make your memory expansion module completely compatible with KIM-1. By setting the switches on the

memory expansion board, you can select the address locations in memory where you wish your expansion memory to reside.

The integrated circuit memories used on your board are high-speed static memory modules. No refresh cycles are required and access to this memory will not require any slow-down of your KIM-1.

Chapter 2 of this manual explains how to install your new memory expansion module in your KIM system. Chapter 3 explains how to check out your memory expansion module and how to test it if you ever suspect that it has failed. Chapter 4 contains information on your memory expansion module warranty, and Chapter 5 explains the theory of operation. If for any reason you are unable to get your memory expansion module operating satisfactorily, follow carefully the checkout instructions in Chapter 3. If you are still unable to get satisfactory operation, return the module as described in Chapter 4 or contact the manager of KIM Customer Support at MOS Technology, Inc. corporate headquarters, 950 Rittenhouse Road, Norristown, PA 19401.

Figure 1

CHAPTER 2

Installation

2.1 INTRODUCTION

How you install your KIM memory expansion module will depend on whether or not you are using a KIM-4 motherboard to interface your expansion module to KIM-1. The pin configuration on your KIM-3B allows you to plug your memory expansion module directly into the KIM-4 motherboard and begin operation immediately. You may insert as many KIM-3B memory expansion modules into the motherboard as you wish, taking care that each is set to a different memory location. If, however, you are connecting your memory expansion module directly to KIM-1, only one KIM-3B may be connected in this manner. In this case you will have to wire a cable for your memory expansion module which connects to the KIM-1 expansion and application connectors. (See Figure 1)

2.2 CONNECTING YOUR MEMORY EXPANSION MODULE TO THE MOTHERBOARD (KIM-4)

If you have already installed a KIM-4 motherboard in your KIM system, it is only necessary to plug the KIM-3B into any slot on the motherboard. Make sure that your motherboard power supply has sufficient capacity to supply the needs of your memory expansion module. See your KIM-4 User Manual for power supply connections. The KIM-3B memory expansion module draws 2.1A maximum. Your KIM memory expansion module should be inserted in the motherboard so that the component side of the board faces away from the end of the motherboard to which KIM-1 is connected. Prior to inserting the memory board in the motherboard set the address switches located on the memory board to the correct position

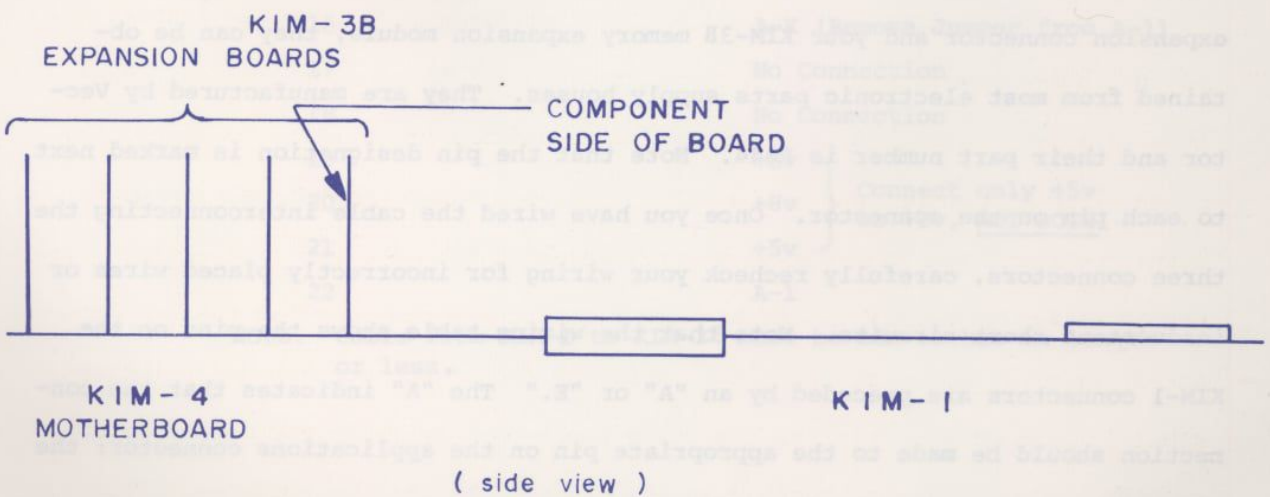
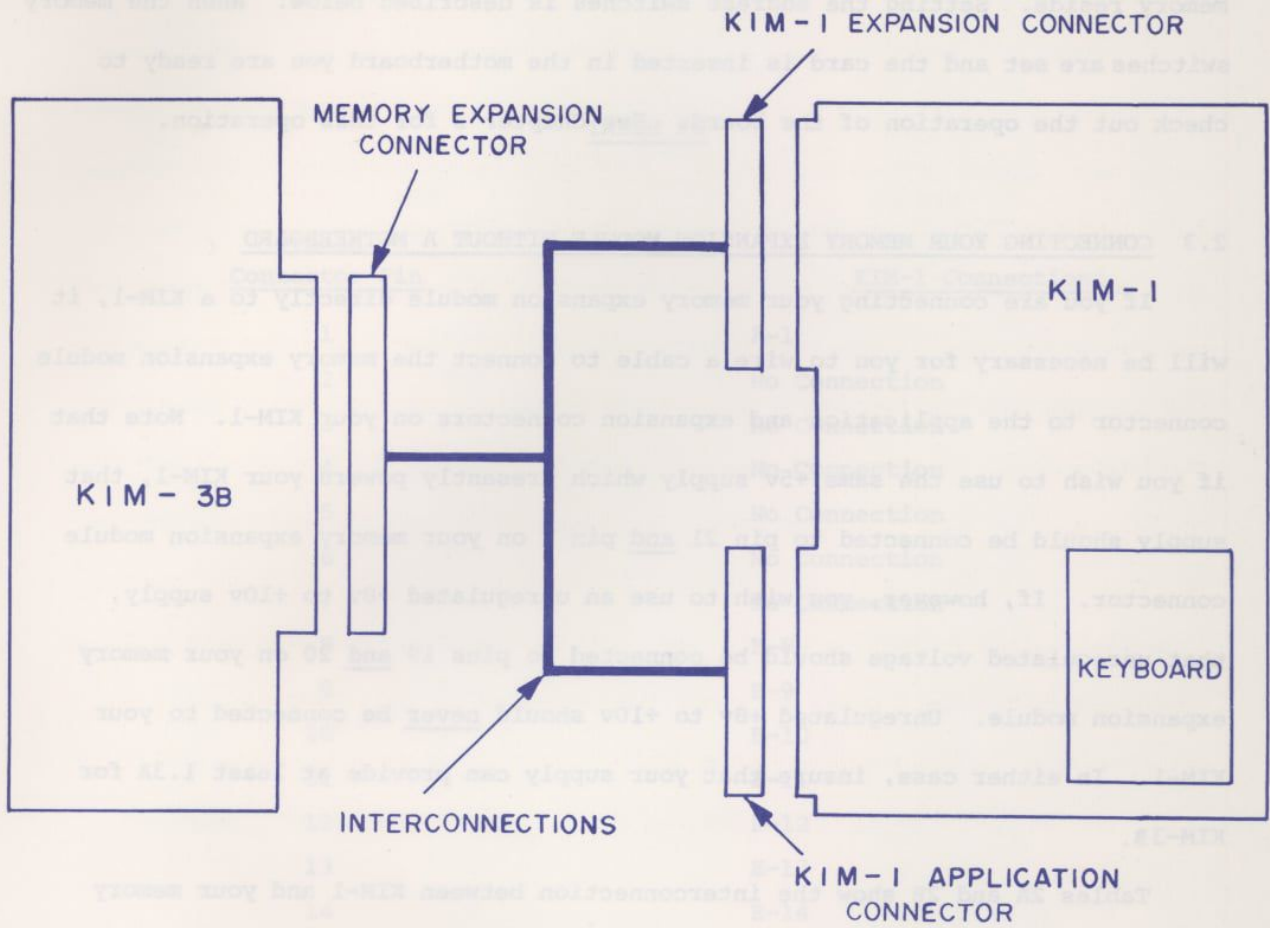


Figure 1

for the address in KIM's memory space where you wish to have the additional memory reside. Setting the address switches is described below. When the memory switches are set and the card is inserted in the motherboard you are ready to check out the operation of the board. See Chapter 3 for this operation.

2.3 CONNECTING YOUR MEMORY EXPANSION MODULE WITHOUT A MOTHERBOARD

If you are connecting your memory expansion module directly to a KIM-1, it will be necessary for you to wire a cable to connect the memory expansion module connector to the application and expansion connectors on your KIM-1. Note that if you wish to use the same +5v supply which presently powers your KIM-1, that supply should be connected to pin 21 and pin Y on your memory expansion module connector. If, however, you wish to use an unregulated +8v to +10v supply, that unregulated voltage should be connected to pins 19 and 20 on your memory expansion module. Unregulated +8v to +10v should never be connected to your KIM-1. In either case, insure that your supply can provide at least 1.3A for KIM-3B.

Tables 2A and 2B show the interconnection between KIM-1 and your memory expansion module. If you do not have the appropriate connectors for the KIM-1 expansion connector and your KIM-3B memory expansion module, they can be obtained from most electronic parts supply houses. They are manufactured by Vector and their part number is R644. Note that the pin designation is marked next to each pin on the connector. Once you have wired the cable interconnecting the three connectors, carefully recheck your wiring for incorrectly placed wires or inadvertent short circuits. Note that the wiring table shows the pins on the KIM-1 connectors are preceded by an "A" or "E." The "A" indicates that the connection should be made to the appropriate pin on the applications connector; the "E" indicates that the pin is on the expansion connector.

3.4 SETTING THE ADDRESS SWITCHES

In order to make your memory expansion module as versatile as possible, we have included four switches to allow you to place your expansion memory at any memory address (see Figure 3). We want you to place your first memory expansion module starting at address 200 hex and continue to expand your memory into successive memory locations.

TABLE 2A

<u>KIM-3B</u> <u>Connector Pin</u>	<u>KIM-1 Connections</u>
1	A-1
2	No Connection
3	No Connection
4	No Connection
5	No Connection
6	No Connection
7	No Connection
8	E-8
9	E-9
10	E-10
11	E-11
12	E-12
13	E-13
14	E-14
15	E-15
16	A-K (Remove Jumper from A-1)
17	No Connection
18	No Connection
19	+8v
20	+8v
21	+5v
22	A-1

} Connect only +5v
or +8v, NOT BOTH

NOTE: Cable from KIM-1 to KIM-3B must be six inches in length or less.

TABLE 2B

<u>KIM-3B Connector Pins</u>	<u>KIM-1 Connections</u>
A	A-1
B	E-A
C	E-B
D	E-C
E	E-D
F	E-E
H	E-F
J	E-H
K	E-J
L	E-K
M	E-L
N	E-M
P	E-N
R	E-P
S	E-R
T	E-S
U	E-T
V	E-U
W	E-V
X	E-Y
Y	To +5v (If +8v NOT USED)
Z	A-1

2.4 SETTING THE ADDRESS SWITCHES

In order to make your memory expansion module as versatile as possible, we have included four switches to allow you to place your expansion memory at any memory address (see Figure 3). We suggest that you place your first memory expansion module starting at address 2000_{hex} and continue to expand your memory into successively higher memory locations. Tables 4 and 5 indicate the switch settings for various memory locations using your KIM-3B. Be sure to consult the appropriate table for the module you have purchased. Once you have chosen the memory space for your expansion module and correctly set the addressing switches, turn off all power and insert the memory module in its connector. You are now ready to test your memory expansion module.

Note: Do not set the switches so that your expansion memory has an address below 2000_{hex} as it will conflict with the memory and other circuitry in your KIM-1. It is not possible to put your expansion memory in the Memory block 0400-1400_{hex} already decoded on KIM-1.

In order to make your memory expansion module as versatile as possible, we have included four switches to allow you to place your expansion memory at any memory address (see Figure 4). We suggest that you place your first memory expansion module starting at address 0000 and continue to expand your memory into successively higher addresses.

KIM-3B Address Switch Setting

When Address Switch Is: Lowest Address Is: Highest Address Is:

<u>3</u> <u>2</u> <u>1</u>			
0 0 0	0000		1FFF (do not use)
0 0 X	2000		3FFF
0 X 0	4000		5FFF
0 X X	6000		7FFF
X 0 0	8000		9FFF
X 0 X	A000		BFFF
X X 0	C000		DFFF
X X X	E000		FFFF

X = Switch is NOT on

0 = Switch IS on

Note: Switch 4 will logically disconnect the board when closed. Switch 5 is used for write protection when left open.

CHAPTER 3

Checkout and Test Program

3.1 Your memory expansion module has been carefully tested to assure correct operation. In this section we will describe how you can briefly check the operation of your memory expansion module. We have also included a test program which will allow you to verify correct operation of all memory cells in your memory expansion module. It should only be necessary to run this program if you suspect that the memory module has failed.

To verify that your memory expansion module has been correctly wired and that the address switches are correctly set, just address some of the memory locations and verify that you can change the contents of those locations. Using the keypad provided with your KIM-1, and assuming that you have set the address switches on your memory expansion module so that the lowest address is 2000, use the following procedure:

Checkout and Test Program

<u>Depress Key</u>	<u>See Displayed</u>
<u>RS</u>	XXXX XX
<u>AD</u>	XXXX XX
<u>2</u> <u>0</u> <u>0</u> <u>0</u>	2000 XX
<u>DA</u>	2000 XX
<u>3</u> <u>A</u>	2000 3A
<u>7</u> <u>9</u>	2000 79
<u>+</u>	2001 XX
<u>3</u> <u>7</u>	2001 37

If you are unable to change the data in memory there are two possible sources of trouble:

1. The memory expansion board is not correctly connected to KIM-1. If you are using a motherboard, check that the motherboard is correctly installed and that the memory expansion card has the component side of the board facing away from the KIM-1. If you are not using a motherboard, carefully check your wiring against the list provided in Tables 2A and 2B.
2. You have incorrectly set the memory address switches. The figure below shows the appearance of the memory address switch when it is configured so that the lowest expansion memory address is 2000_{16} . Recheck the information in Chapter 2 if you are unsure of the placement of the memory expansion module.

3.2 TEST PROGRAM FOR MEMORY CHECKOUT

Although your KIM memory expansion module has been carefully tested before shipment, like any other electronic device, it can fail in use. If you suspect that your memory expansion module is not working correctly, the following program can be used to check the memory operation. It should be noted that programs for testing memory modules for all possible failure modes would be quite complex and require lengthy running time on KIM. The following programs simply write and read every possible bit pattern in every memory location. They do not check, for instance, whether writing to a given memory location may also affect other memory locations.

3.3 CHECKING YOUR MEMORY FROM A TERMINAL

The following program assumes that you have a terminal connected to the serial input and output ports of your KIM-1. To use the program, type it into KIM memory starting at location 200₁₆; make a paper tape copy once you have loaded the program using the KIM dump routine. To operate the program, load the lowest address which you wish to test in location 0000 and 0001, then load the highest memory address you wish to test in location 0002 and 0003. For instance, to check all memory locations between 2000 and 2FFF you would load 00 in location 0000, 20 in location 0001, FF in location 0002, and 2F in location 0003. To operate the program, load address 022A and hit the G key. The program will then fill the specified memory locations with 0's and then read all locations to verify that the zero has been written. It will then load the specified memory with 01 and again verify the data. The process will continue until all bit patterns from 00 to FF have been written and read correctly. If any memory location fails to read or write correctly the address of the defective cell will be written to the terminal, along with the code which would not

Program 1

CARD =	LOC	CODE	CARD
1			BOTLO=\$0
2			BOTHI=\$1
3			TOPLO=\$2
4			TOPHI=\$3
5			PTRLO=\$4
6			PTRHI=\$5
7			MASK=\$6
8			PRTBYT=\$1E3B
9			OUTSP=\$1E9E
10			CRLF=\$1E2F
11	0000		*=\$200
12	0200	E6 04	INCPTR INC PTRLO
13	0202	D0 02	BNE END
14	0204	E6 05	INC PTRHI
15	0206	60	END RTS
16			
17			ERROR ROUTINE FOR TTY
18			
19	0207	A5 05	ERROR LDA PTRHI
20	0209	20 3B 1E	JSR PRTBYT
21	020C	A5 04	LDA PTRLO
22	020E	20 3B 1E	JSR PRTBYT
23	0211	20 9E 1E	JSR OUTSP
24	0214	A5 06	LDA MASK
25	0216	20 3B 1E	JSR PRTBYT
26	0219	20 2F 1E	JSR CRLF
27	021C	60	RTS
28			
29			INITIALIZATION SUBROUTINE
30			
31	021D	A9 00	INIT LDA =\$00
32	021F	85 06	STA MASK
33	0221	A5 00	RESET LDA BOTLO
34	0223	85 04	STA PTRLO
35	0225	A5 01	LDA BOTHI
36	0227	85 05	STA PTRHI
37	0229	60	RTS
38			
39			MAINLINE FOR MEMORY TEST
40			
41	022A	D8	BEGIN CL)
42	022B	20 1D 02	JSR INIT
43	022E	A0 00	LP1 2DY #\$00
44	0230	A5 06	WRLOOP LDA MASK
45	0232	91 04	STA (PTRLO),Y
46	0234	20 00 02	JSR INCPTR
47	0237	A5 04	LDA PTRLO
48	0239	C5 02	CMP TOPLO
49	023B	D0 F3	BNE WRLOOP
50	023D	A5 05	LDA PTRHI
51	023F	C5 03	CMP TOPHI
52	0241	D0 ED	BNE WRLOOP
53	0243	20 21 02	JSR RESET
54	0246	B1 04	RDLOOP LDA (PTRLO),Y
55	0248	C5 06	CMP MASK
56	024A	F0 03	BEQ CONT
57	024C	20 07 02	JSR ERROR
58	024F	20 00 02	CONT JSR INCPTR
59	0252	A5 04	LDA PTRLO
60	0254	C5 02	CMP TOPLO
61	0256	D0 EE	BNE RDLOOP
62	0258	A5 05	LDA PTRHI
63	025A	C5 03	CMP TOPHI
64	025C	D0 E8	BNE RDLOOP
65	025E	E6 06	INC MASK
66	0260	D0 03	BNE CYCLE
67	0262	20 2F 1E	JSR CRLF
68	0265	20 21 02	CYCLE JSR RESET
69	0268	4C 2E 02	JMP LP1

END OF MOS/TECHNOLOGY 650X ASSEMBLY VERSION 4
 NUMBER OF ERRORS = 0, NUMBER OF WARNINGS = 0

read or write correctly. When all bit patterns have been tested in all specified cells, the program will output a carriage return and line feed and begin the entire cycle over again. For a 4K memory expansion module the entire test will take about 1-1/2 minutes.

3.4 CHECKING MEMORY OPERATION WITH THE KEYPAD

Program 2 tests memory in a similar fashion, but does not require a terminal. As in the first program, the address of the lower limit and upper limit of the memory to be checked is inserted in locations 0 through 3. When the program has been keyed in, you will probably wish to record it on your audio cassette for future use. When the starting address (022E) is loaded and the GO button is depressed the program will check memory as described above. However, if a defective cell is encountered the address of the defective cell will be displayed on the leftmost four digits of the display and the program will halt. Pushing any button on the keypad will resume the testing operation. When all memory cells have been checked, a value of 0000 will appear in the display and the program will halt.

Program 2

CARD = LOC	CODE	CARD
1		BOTLO=\$0
2		BOTHI=\$1
3		TOPLO=\$2
4		TOPHI=\$3
5		PTRLU=\$4
6		PTRHI=\$5
7		MASK=\$6
8		POINTH=\$FB
9		POINTL=\$FA
10		SCANS=\$1F1F
11		AK=\$1EFE
12		RESVEC=\$1C22
13	0000	*=\$200
14	0200 E6 04	INCPTR INC PTRLO
15	0202 D0 02	BNE END
16	0204 E6 05	INC PTRHI
17	0206 60	END RTS
18		
19		ERROR ROUTINE FOR KEYPAD
20		
21	0207 A5 05	ERROR LDA PTRHI
22	0209 85 FB	STA POINTH
23	020B A5 04	LDA PTRLO
24	020D 85 FA	STA POINTL
25	020F A5 06	LDA MASK
26	0211 85 F9	STA \$F9
27	0213 20 1F 1F	ER1 JSR SCANS
28	0216 20 FE 1E	JSR AK
29	0219 F0 F8	BEQ ER1
30	021B 20 FE 1E	ERLOOP JSR AK
31	021E D0 FB	BNE ERLOOP
32	0220 60	RTS
33		
34		INITIALIZATION SUBROUTINE
35		
36	0221 A9 00	INIT LDA =\$00
37	0223 85 06	STA MASK
38	0225 A5 00	RESET LDA BOTLO
39	0227 85 04	STA PTRLO
40	0229 A5 01	LDA BOTHI
41	022B 85 05	STA PTRHI
42	022D 60	RTS
43		
44		MAINLINE FOR MEMORY TEST
45		
46	022E D8	BEGIN CLD
47	022F A0 00	LDY =\$00
48	0231 20 21 02	JSR INIT
49	0234 A5 06	WRLOOP LDA MASK
50	0236 91 04	STA (PTRLO),Y
51	0238 20 00 02	JSR INCPTR
52	023B A5 04	LDA PTRLO
53	023D C5 02	CMP TOPLO
54	023F D0 F3	BNE WRLOOP
55	0241 A5 05	LDA PTRHI
56	0243 C5 03	CMP TOPHI
57	0245 D0 ED	BNE WRLOOP
58	0247 20 25 02	JSR RESET
59	024A B1 04	RDLOOP LDA (PTRLO),Y
60	024C C5 06	CMP MASK
61	024E F0 03	BEQ CONT
62	0250 20 07 02	JSR ERROR
63	0253 20 00 02	CONT JSR INCPTR
64	0256 A5 04	LDA PTRLO
65	0258 C5 02	CMP TOPLO
66	025A D0 EE	BNE RDLOOP
67	025C A5 05	LDA PTRHI
68	025E C5 03	CMP TOPHI
69	0260 D0 E8	BNE RDLOOP
70	0262 E6 06	INC MASK
71	0264 D0 09	BNE LOOP
72	0266 A9 00	LDA =\$00
73	0268 85 FA	STA \$FA
74	026A 85 FB	STA \$FB
75	026C 4C 22 1C	JMP RESVEC
76	026F 20 25 02	LOOP JSR RESET
77	0272 4C 34 02	JMP WR LOOP
78		.END

CHAPTER 4

Warranty and Service

Should you experience difficulty with your KIM-3B module and be unable to diagnose or correct the problem, you may return the unit to MOS Technology, Inc. for repair.

4.1 IN-WARRANTY SERVICE

All KIM series microcomputer modules are warranted by MOS Technology, Inc. against defects in workmanship and materials for a period of ninety (90) days from date of delivery. During the warranty period, MOS Technology, Inc. will repair or, at its option, replace at no charge components that prove to be defective provided that the module is returned, shipping prepaid, to:

KIM Customer Service Department
901 California Ave.
Palo Alto, CA 94304

This warranty does not apply if the module has been damaged by accident or misuse, or as a result of repairs or modifications made by other than authorized personnel at the above captioned service facility.

No other warranty is expressed or implied. MOS Technology, Inc. is not liable for consequential damages.

4.2 OUT-OF-WARRANTY SERVICE

Beyond the ninety (90) day warranty period, KIM modules will be repaired for a reasonable service fee. All service work performed by MOS Technology,

Inc. beyond the warranty period is warranted for an additional ninety (90) day period after shipment of the repaired module.

4.3 POLICY OF CHANGES

All KIM series modules are sold on the basis of descriptive specifications in effect at the time of sale. MOS Technology, Inc. shall have no obligation to modify or update products once sold. MOS Technology, Inc. reserves the right to make periodic changes or improvements to any KIM series module.

4.4 SHIPPING INSTRUCTIONS

It is the customer's responsibility to return the KIM series module with shipping charges prepaid to the above captioned service facility.

For in-warranty service, the KIM module will be returned to the customer, shipping prepaid, by the fastest economical carrier.

For out-of-warranty service, the customer will pay for shipping charges both ways. The repaired KIM module will be returned to the customer C.O.D. unless the repairs and shipping charges are prepaid by the customer.

Please be certain that your KIM module is safely packaged when returning it to the above captioned service facility.

CHAPTER 5

Theory of Operation

5.1 The schematic shows the interconnection of the components on the KIM-3B board. The diagram below illustrates the pin connections to the 2114-type memories used on the boards. When \overline{CSX} is low, four of the 1024 bits in the package are selected. If \overline{WE} is low, the selected cells will have the values of the I/O lines (1 or 0) written into them. If pin \overline{WE} is high, the contents of the addressed cells will be placed on the I10 lines.

6550			
A6	1	18	VCC
A5	2	17	A7
A4	3	16	A8
A3	4	15	A9
A0	5	14	I/01
A1	6	13	I/02
A2	7	12	I/03
\overline{CS}	8	11	I/04
GND	9	10	\overline{WE}

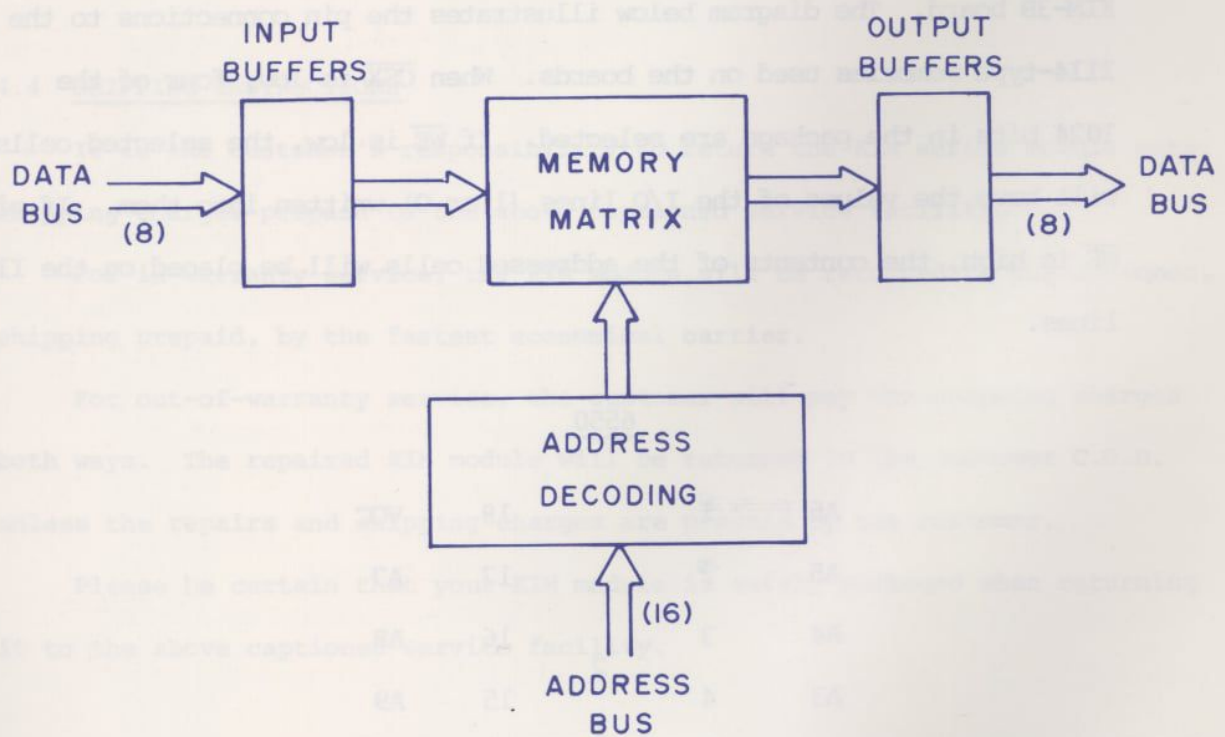
The board is composed of the memory circuits, addressing circuitry, and buffers. An on-board voltage regulator is also provided.

In operation, address bus lines 0 through 9 are buffered by A10, B10 and B11, and connected directly to the memory circuits. The high-order address

The layout of the memory circuit is shown in Figure 4.3. The memory circuit is connected to the data bus and the address bus. The memory circuit is connected to the data bus through input and output buffers. The memory circuit is connected to the address bus through an address decoder.

4.3 MEMORY CIRCUIT

The memory circuit is connected to the data bus and the address bus. The memory circuit is connected to the data bus through input and output buffers. The memory circuit is connected to the address bus through an address decoder.



The diagram shows the memory circuit connected to the data bus and the address bus. The memory circuit is connected to the data bus through input and output buffers. The memory circuit is connected to the address bus through an address decoder.

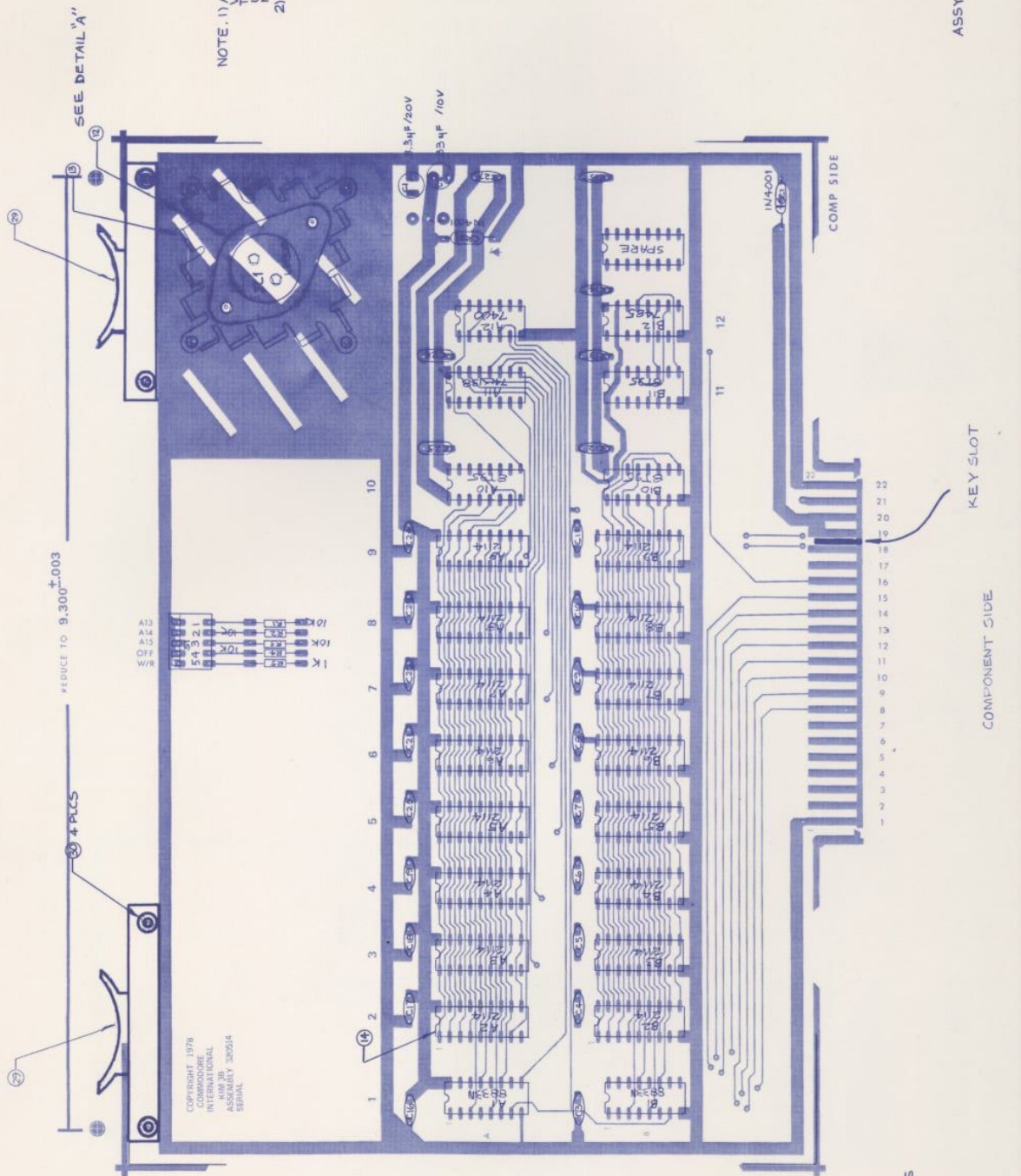
The diagram shows the memory circuit connected to the data bus and the address bus. The memory circuit is connected to the data bus through input and output buffers. The memory circuit is connected to the address bus through an address decoder.

lines (A13 - 15) are presented to B12, a 4-bit comparator. The bit pattern on these lines is compared with the bit pattern generated by the three address switches. If the address switch settings and the high-order address lines match, pin 6 of B12 will go high. This signal is passed off the board as the board SELECTED line (BDSEL). When BDSEL goes high it disables U4 on KIM-1, preventing the memory circuits on KIM-1 from conflicting with addresses intended for the expansion memory board.

Address bus lines 10, 11 and 12 are decoded in A11 to provide eight output lines. Each of these eight lines is connected to two memory circuits to determine which memory will be active at any time. The memory circuits will not be activated unless the proper address configuration exists on address bus lines 13, 14 and 15. The comparison signal from pin 6 of B12 is also used in A12 to combine with the $\phi 2$ and R/W signals from KIM-1 to control the input and output buffers (A1 and B1).

When clock phase 2 is present the data bus buffers will be enabled, allowing data to be fed into or out of the board, depending on the condition of the Read/Write line. A11 will enable the appropriate two memory circuits and the selected memory circuits will decode the ten least significant address bits to complete the Read/Write operation.

Also present is a conventional 3-terminal regulator, which takes the unregulated +8v supplied to the board and supply a regulated +5v for the circuitry.

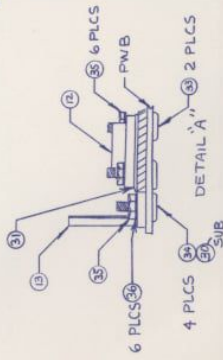


NOTE. 1) ALL RESISTOR VALUES IN OHMS, UNLESS OTHERWISE NOTED. OTHERWISE NOTED.
 2) ALL CAPACITORS ARE .1 MICROFARAD, 10 VOLT, UNLESS NOTED.

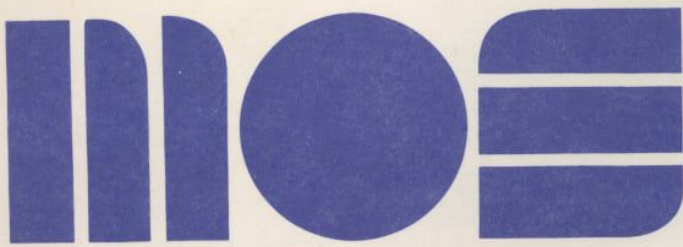
REDUCE TO 9.300±.003

SEE DETAIL A

COPYRIGHT 1978
 INTERNATIONAL
 MINI PC
 ASSEMBLY 306914
 SERIAL



ASSY, PCB, KIM 3B



MOST TECHNOLOGY, INC.

VALLEY FORGE CORPORATE CENTER

950 RITTENHOUSE ROAD, NORRISTOWN, PA. 19401

TEL: (215) 666-7950

TWX: 510/660/4033
